IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/924,856
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Inventorship.....Hampel et al.
Applicant.....Rambus Inc.
Group Art Unit 2818
Examiner .....Trong Q. Phan
Attorney's Docket No. RB1-037USC1
Title: Method And Apparatus For Reducing Worst Case Power

RESPONSE TO OFFICE ACTION DATED (MAILED) 10/29/2002

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

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AMENDMENTS

In The Specification

Please replace the fourth paragraph (beginning at line 15) of page 23 with the following:

For one embodiment, address bit A_0 is also used to generate the ALT signal on line 855 and 1118 that is applied as an input to XOR gates 810, 812, 1108, and 1110. For one embodiment, the address rate on lines 853 and 1118 is the same rate as the data rate on lines 818. The address bit A_0 toggles at the maximum rate of the addresses and thus functions also as the ALT signal for the reformatting circuitry.